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This paper presents the way of speeding up the route from the theoretical design with Simulink/Matlab, via behavioral simulation

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from the theoretical design with Simulink/Matlab, via behavioral simulation in fixed-point arithmetic to the implementation on either FPGA or custom

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silicon. This has been achieved by porting the netlist of the Simulink system description into the VHDL. At the first instance, the Simulink-to-VHDL converter has been designed to use

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I have a complete project where I use MATLAB coding in S-function Level 2 as well as Simulink blocks. I would like to convert the above project into Verilog or VHDL (I can choose but I don't know which one is better for the moment) to be implemented on a hardware FPGA design on DE0 Nano Development board.



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## **MATLAB: How to convert Simulink project into Verilog or ...**

At the first instance, the Simulink-to-VHDL converter has been designed to use structural VHDL code to describe system interconnections, allowing simple behavioral descriptions for basic blocks. The resulting VHDL code delivers bit-true result when compared to the

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design on DE0 Nano  
Development board.

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Rapid  
HDL Code Generation  
for Any Target. Use  
high-level synthesis  
techniques to compile  
hardware-ready  
MATLAB or Simulink to  
readable, traceable,  
and synthesizable  
VHDL or Verilog HDL  
code. This code is  
optimized and portable

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across any FPGA, ASIC,  
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quality HDL code  
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experience.

## **Simulink for HDL Code Generation - MATLAB & Simulink**

Specify the format for  
saving simulation  
output to the  
workspace. The default  
Timeseries format  
saves nonbus signals

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as a MATLAB  
timeseries object and  
bus signals as a  
structure of MATLAB  
timeseries objects..

The Array format saves  
the input as an N-  
dimensional array  
where N is one more  
than the number of  
dimensions of the input  
signal.

## **Write data to workspace - MATLAB & Simulink**

The derived VHDL

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model will consist of a combination of behavioural, RTL and structural definitions mapped directly from the Simulink model. This approach may enable a user to develop and simulate a digital control algorithm using Mat/ab and once complete, convert this to VHDL code.

## **A MATLAB to VHDL Conversion Toolbox**

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This paper presents the way of speeding up the route from the theoretical design with Simulink/Matlab, via behavioral simulation in fixed-point arithmetic to the implementation on either FPGA or custom silicon. This has been achieved by porting the netlist of the Simulink system description into the VHDL.



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if you have  
Synthesizable subset of  
verilog you can import  
into Simulink using  
"importhdl"  
functionality. We do  
not yet support VHDL.  
if you can please share  
your sample design  
with us [kiran.kintali@m  
athworks.com](mailto:kiran.kintali@mathworks.com)

**Import VHDL in**

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Following VHDL code generation, we must prepare the code for hardware implementation. To do this we synthesize the VHDL code that we generated for the first stage of the filter and perform place and route for a Virtex 4 vsx25-10 FPGA using Xilinx ISE software tools. The timing

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analysis shows that we  
can run the design at a  
clock rate of 210 MHz.  
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HDL Verifier™ reuses  
your MATLAB and

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## **How can MATLAB code be converted to VHDL code?**

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way of speeding up the route from the theoretical design with Simulink/Matlab, via behavioral simulation in fixed-point arithmetic to the implementation on either FPGA or custom silicon.

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